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FOUR-FREQUENCY RADAR MASTER CONSOLE

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ABSTRACT

In conjunction with the commercially contracted development of the airborne four-frequency radar system to be used in the Laboratory's wave propagation studies, the master console design was assumed by NRL. Four displays were incorporated into a single console, along with transmitter, receiver, and antenna drive control functions. Two cathode-ray tubes present the PPI and B scans, while a third presents dual traces representing linear A sweeps. The system-control-panel-assembly portion of the master console was completed on schedule to assist the contractor in the radar development. The rest of the console was designed and completed so as to meet the contractor's schedule for system tests. Video circuit bandwidth requirements of 10 Mc and sweep ranges from 1/4 mile up to 200 miles were met in the critical A-scope circuitry.

PROBLEM STATUS

The main console portion of the problem has been completed. Other portions of the problem, including the development of consoles 2 and 3, are continuing in this Branch.

AUTHORIZATION

NRL Problem R07-02
Project RR 008-01-41-5550

Manuscript submitted January 24, 1963.

FOUR-FREQUENCY RADAR MASTER CONSOLE

INTRODUCTION

Background

In conjunction with the commercially contracted development of the airborne four-frequency radar system to be used in the Laboratory's wave propagation studies, the master console design was assumed by NRL. Four displays were to be incorporated into a single console, along with transmitter, receiver, and antenna drive control functions. Two cathode-ray tubes would present the PPI and B scans, while a third would present dual traces representing linear A sweeps for horizontally and vertically polarized signals. The control facilities required included the choices of transmitter frequency, repetition rate, pulse length, polarization, and antenna scan rate, magnitude, and bearing. A target tracking gate control and a range-gate readout having a decimal-digital display, were specified. The Data Processing Branch assumed the responsibility for the completion and delivery of the console, with delivery dates to meet the contractor's schedule for system tests.

Accomplishments

The system-control-panel assembly is a separate unit on top of the master console. It was assembled and wired as specified by the contractor in order to meet the specified June 1, 1962, delivery date. In the display portions of the console, bandwidth requirements of 10 Mc were met by the video amplifiers. Extended sweep ranges of from 1/4 mile up to 200 miles were incorporated into the master console.

During shipment to the contractor's plant, a fire of unknown origin started in the packing material. Following return to NRL, emergency measures were initiated, with material and manpower assistance from the Chemistry Division, for the cleaning, renovating, repair, and repainting of the damaged areas. Delivery to the contractor was completed six working days after the originally scheduled date.

CIRCUIT DIAGRAMS

Function Diagram

The master-console function diagram is shown in Fig. 1. The trigger pulse lines T_1, T_2, T_3, and T_4 terminate with 91-ohm resistors and drive the four-frequency-selector switches for the PPI, A1, A2, and B cathode-ray-tube displays. The four trigger pulses are also combined in the 1N916 diode "or" circuit, the output of which is delayed by the variable delay circuit, then drives the normal sweep generator. The outputs of the frequency selector switches go to the corresponding cathode-ray-tube (crt) unblanking chassis. The delayed trigger line, upon which all delayed triggers come in sequence from the radar synchronizer, pass through the buffer amplifier and to the input of the expanded sweep generator. The output of the buffer amplifier also drives the line to display consoles 2 and 3. The radar polarization signals drive the polarization selector

switches for the four crt displays. The outputs of the polarization selector switches go to the corresponding unblanking circuits. When a display is set to view both polarizations being received by the radar receiver, a dc voltage is applied to the unblanking circuit.

When the console is being operated, the frequency selector switches are set to the desired positions. The trigger pulses drive the time delay circuit through the diode "or" network. The normal sweep generator produces output sweep and sweep period signals for each trigger pulse out of the delay circuit. These signals go to the sweep control chassis, where relays select between the normal and expanded sweep generator outputs for the A_1, A_2, and B displays. The expanded sweep generator is identical to the normal sweep generator except for differences in the sweep lengths available. The expanded sweep generator operates for every delayed trigger present, as only the selected frequency will be unblanked. Since the PPI display does not use the expanded sweep, the normal sweep goes directly to the resolver and the normal sweep period signal goes directly to the PPI unblanking circuit.

The sweep control circuit consists of three double-pole double-throw relays, each controlled from a toggle switch associated with the respective crt displays. The relays direct either the normal or expanded sweep to the corresponding deflection amplifier. At the same time the relay directs the associated sweep period signal to the corresponding unblanking circuit. Thus if the A1 crt sweep control switch was set on the expand position, the expand sweep would drive the A1 deflection amplifier and the expand sweep period signal would be connected to the A1 unblanking circuit, where it acts to blank the display at the end of the sweep period.

The signal from the unblanking circuit is a positive pulse starting at the trigger and stopping at the end of the sweep and is coupled to its corresponding crt grid through a high voltage capacitor. This pulse raises the bias level of the crt and allows the selected sweep period to be brightened on the crt.

The sweep from the normal sweep generator drives the resolver buffer amplifier on the antenna follower chassis. The resolved sweeps then drive the PPI deflection amplifiers. A servo amplifier which follows the radar antenna motion drives the sine potentiometer resolver. The servo input signals are designated as the S1, S2, S3 inputs. An ac servo error signal from the radar antenna is inserted into the antenna follower servo to correct for the dynamic errors of the antenna control servo, which would otherwise degrade the PPI and B-scope displays.

The horizontal deflection of the B-scope is derived from the antenna sawtooth generator which controls the radar antenna drive circuits. A dc error signal and the demodulated ac error signal are summed in the horizontal B-scope deflection amplifier in order to have the displayed radar target intensified at the same point on the crt regardless of whether the antenna is scanning clockwise or counterclockwise. Two error signals are required for the B-scan because the radar antenna drive system has a followup error and the antenna sawtooth generator has an independent followup error. Both of these error signals must be removed from the B-scan deflection so that a target will appear at the same point on the crt as the antenna scans back and forth.

The radar video is derived from two receivers, one each for the horizontally and for the vertically polarized radar returns. The video is processed by the radar system, providing for display the direct and gated video of horizontal and vertical polarization amplitudes, horizontal and vertical phases compared against a local reference, and the relative horizontal versus vertical phase. The video switching provides only the direct ungated video for the PPI and B scopes. The A1 and A2 scopes can be switched to present any of the fifteen video sources from the radar processing equipment.

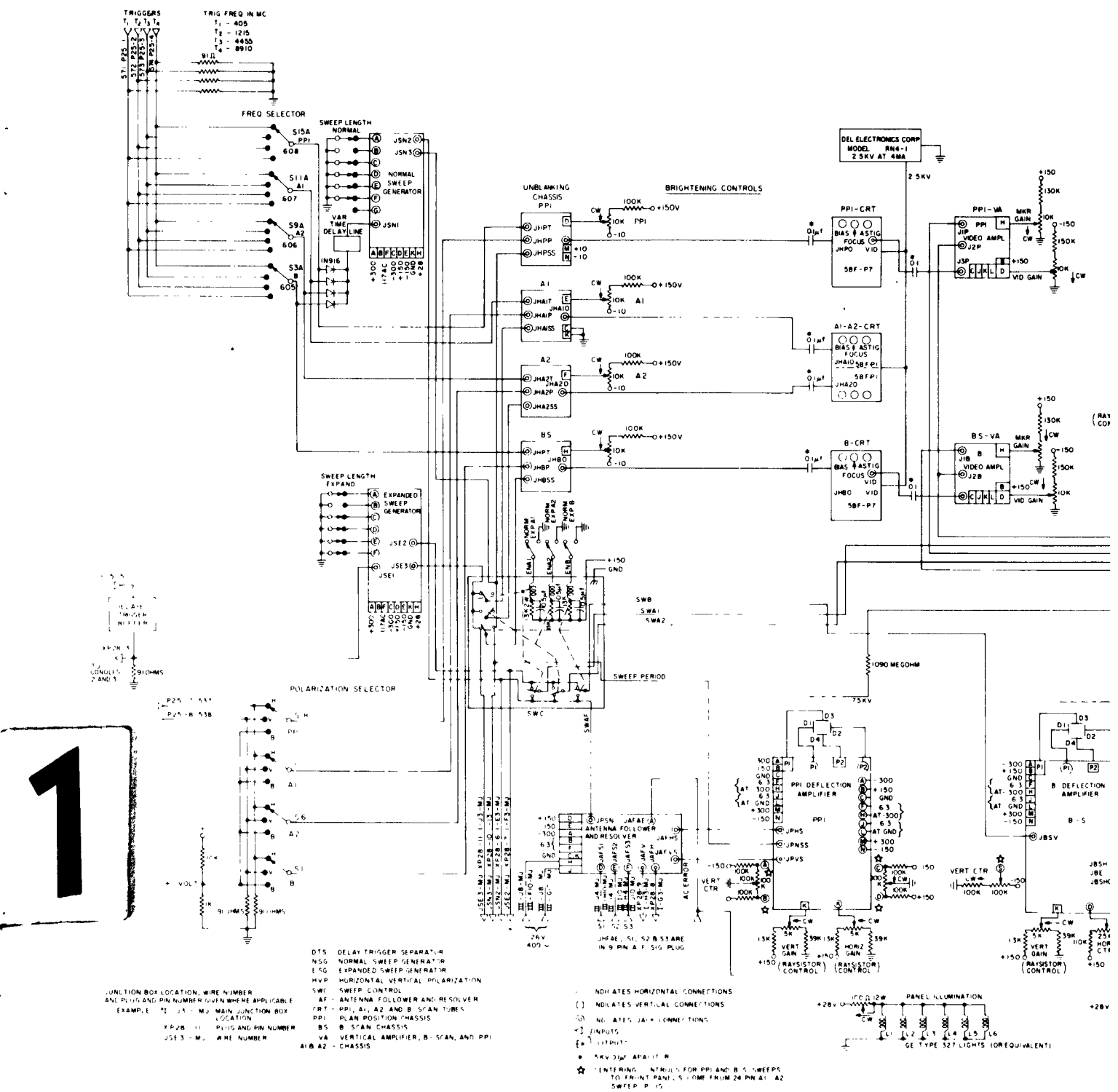
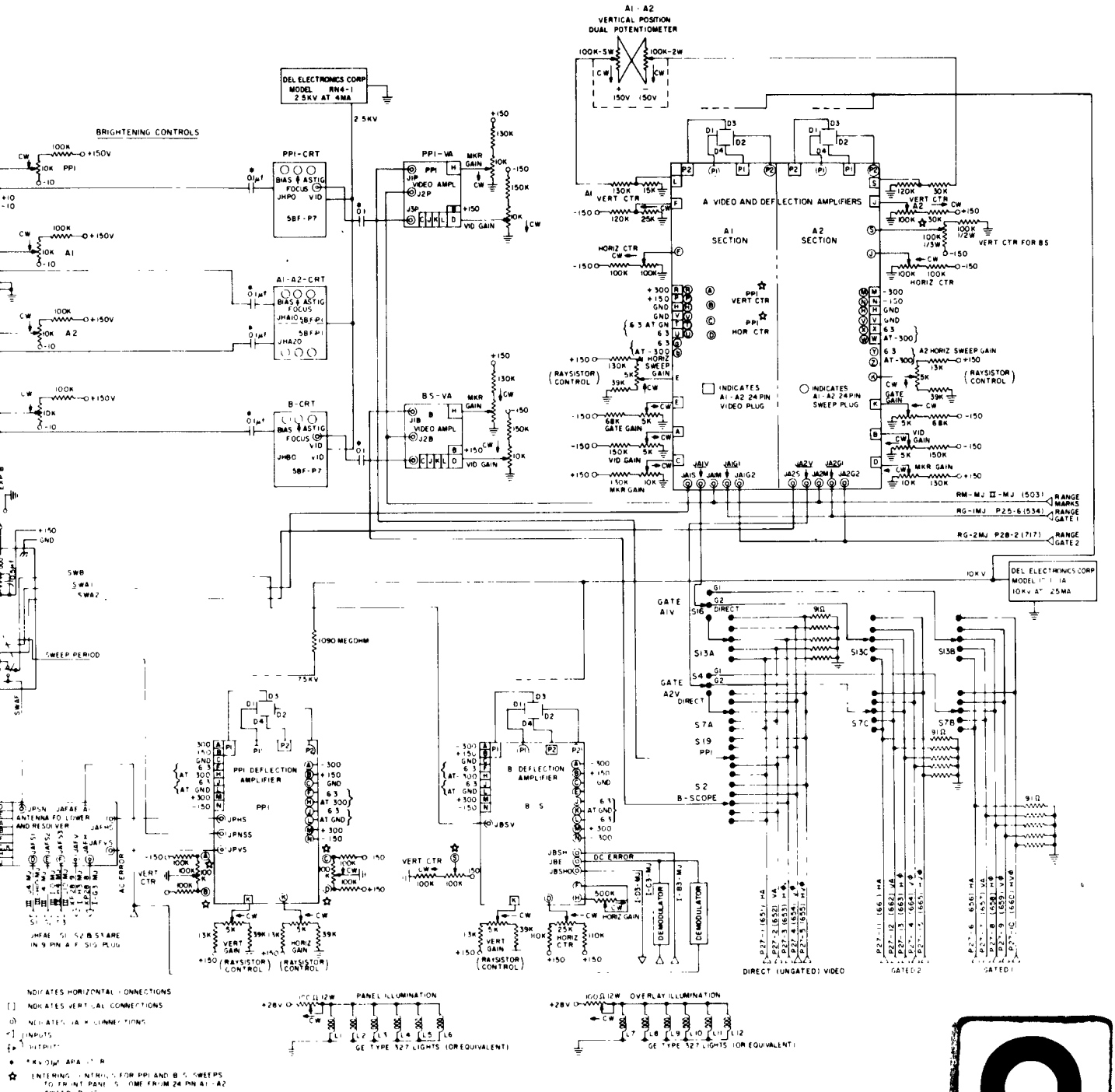


Fig. 1 - Functional wiring diagram of the four-frequency radar maste



Functional wiring diagram of the four-frequency radar master console

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The PPI and B-scope video amplifiers provide a negative output which drives the cathode of these crt displays. Provisions are made to present the range marks through these amplifiers. The A1 and A2 scope video deflection amplifiers provide push-pull output pulses which drive the vertical deflection plates of these crt displays. The range marks are presented with the same polarity as the incoming video. Provisions are made for presenting the two gating period waveforms with either polarity (by minor wiring change) on the A1 and A2 displays.

Figure 1 also includes all of the gain, centering, brightening, delaying, and switching circuits necessary to control the crt displays. The main junction box terminal locations, wire numbers, and plug pin numbers are shown where applicable. The panel and overlay illumination circuits have been included.

Pretrigger Delay Chassis

The trigger signals being supplied by the synchronizer to the master console are from 1 to 2 microseconds ahead of the main triggers. These pretriggers are delayed by the circuit shown in Fig. 2 so that the crt sweeps will start at the correct time with respect to the main triggers. An npn transistor amplifier drives a variable delay line which permits the output to be delayed from 0 to 2.2 μs. The tapped output of the delay line is amplified and drives the input to the normal sweep generator circuit in Fig. 3. The pretrigger delay chassis has a voltage gain between 1 and 2 and with an input pulse having a rise time of 20 nanoseconds (ns) provides an output pulse with a rise time of less than 0.2 microsecond (μs).

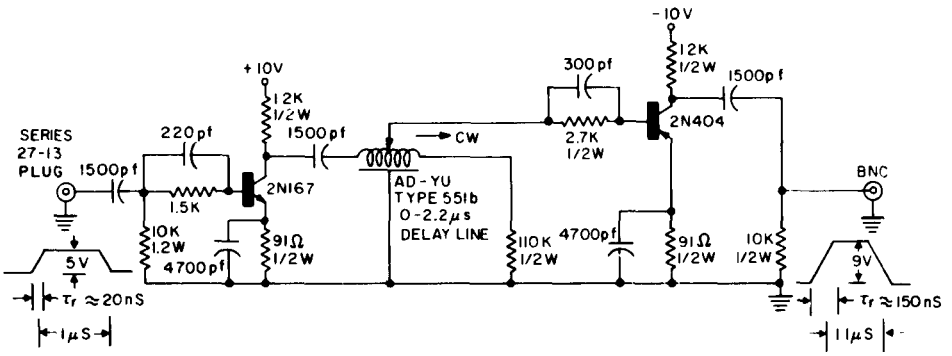

Fig. 2 - Pretrigger delay chassis

Sweep Generator Chassis

The sweep generator chassis shown in Fig. 3 uses a single bootstrap circuit for generating the sweep. The sweep length is changed by a remotely controlled stepping switch which grounds the proper charging capacitor in the sweep circuit. The normal and expanded sweep generators are identical except for the values of the charging capacitors as indicated in Fig. 3.

The trigger input pulse is amplified and inverted by V1A. This pulse sets the flip-flop V4 such that V2 is cut off. The amplified pulse also aids in cutting V2 off faster. With V2 cut off, the selected capacitor (C_a in this case), starts charging positively through the 1-megohm resistor. This waveform appears at the output of V3 as the output sweep

waveform. This signal is bootstrapped back to the 1-megohm charging resistor through a 0.5-μf capacitor. When the sweep starts, the 1N627 diode is cut off by the bootstrap action. During the time that the sweep generator is not operating, the 0.5-μf capacitor is charged through the 1N627 diode from the +300-volt supply. The sweep voltage from V3 is dc coupled to the grid of V1B, which is normally cut off. When the sweep reaches the desired value (as determined by the bias on the grid of V1B), V1B conducts and resets the flip-flop V4 such that V2 is again brought into conduction. The charging capacitor is discharged through V2 and the sweep generator is ready for the next trigger pulse. The positive pulse from the flip-flop is buffered through the cathode follower V5 and becomes the output sweep period signal. This circuit produces a 30-volt-peak-output sweep signal which can be varied from 3-μs duration to 2440-μs duration depending upon the value of the charging capacitor selected. The sweep period output pulse is approximately 40 volts peak.

Unblanking Chassis

The unblanking chassis circuit shown in Fig. 4 provides the necessary unblanking waveform to the crt circuit for brightening the desired sweep periods on the associated display. There is one unblanking chassis for each of the four displays. The operator selects the sweep period by setting the front panel controls to the positions desired. This provides the proper polarization signal, trigger pulse, and sweep period pulse to the unblanking circuit. The selected polarization pulse and selected pretrigger pulse, when viewing the normal sweep period, drive the inputs of the "and" circuit consisting of Q1 and Q6. The polarization pulse is dc coupled because of its long duration. In case both polarizations are chosen to be viewed, the input to Q6 is a dc voltage of +1 volt. When the polarization pulse is at 0 volts, Q6 is cut off, thus allowing Q1 to amplify the trigger pulse and drive the inverting amplifier Q2. The amplified pulse then sets the flip-flop consisting of Q3 and Q4 such that Q3 is cut off. The sweep period pulse is differentiated at the input to Q5 and the trailing edge is amplified by Q5. This amplified pulse resets the flip-flop such that Q3 is made to conduct. The output of Q3, which provides the unblanking period waveform, then drives Q7, which amplifies and inverts the output of Q3. The output of Q7 drives a diode resistor network which provides the means of controlling the amplitude of the unblanking pulse.

The brightness control potentiometer is remotely located from the unblanking chassis, as indicated in Fig. 1. This control provides a dc voltage which keeps the 1N645 diode at the output of Q7 from conducting until the voltage at the collector of Q7 exceeds this dc voltage, thus controlling the brightening pulse amplitude. The dc level is not important because the unblanking pulse is ac coupled to the grid of the crt and dc is restored at that point.

When the expanded sweep is displayed, the circuit above unblanks the crt from the instant of the pretrigger until the end of the expanded sweep period. This causes the crt to be unblanked for the period just preceeding the expanded sweep.

Antenna Follower Chassis

The antenna follower chassis in Fig. 5 provides the servo system for driving a sine-cosine potentiometer which resolves the output of the normal sweep generator for the PPI display. The servo amplifier is a plug-in integrator servo amplifier from an AN/SPS-T2 radar trainer. A half-wave rectifier provides the -28 volts dc for the servo drive transistors.

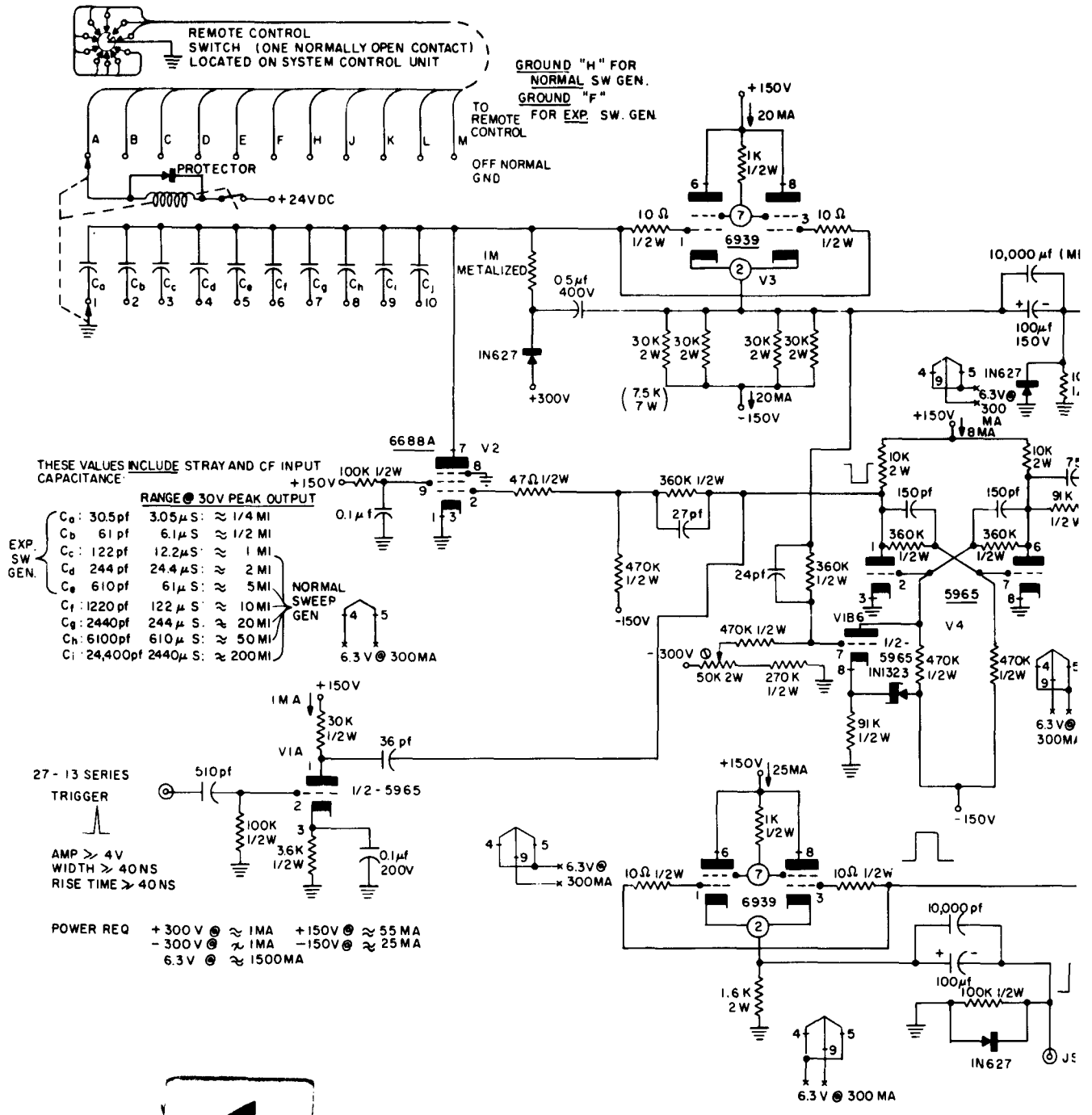

Fig. 3 - Sweep generator chassis

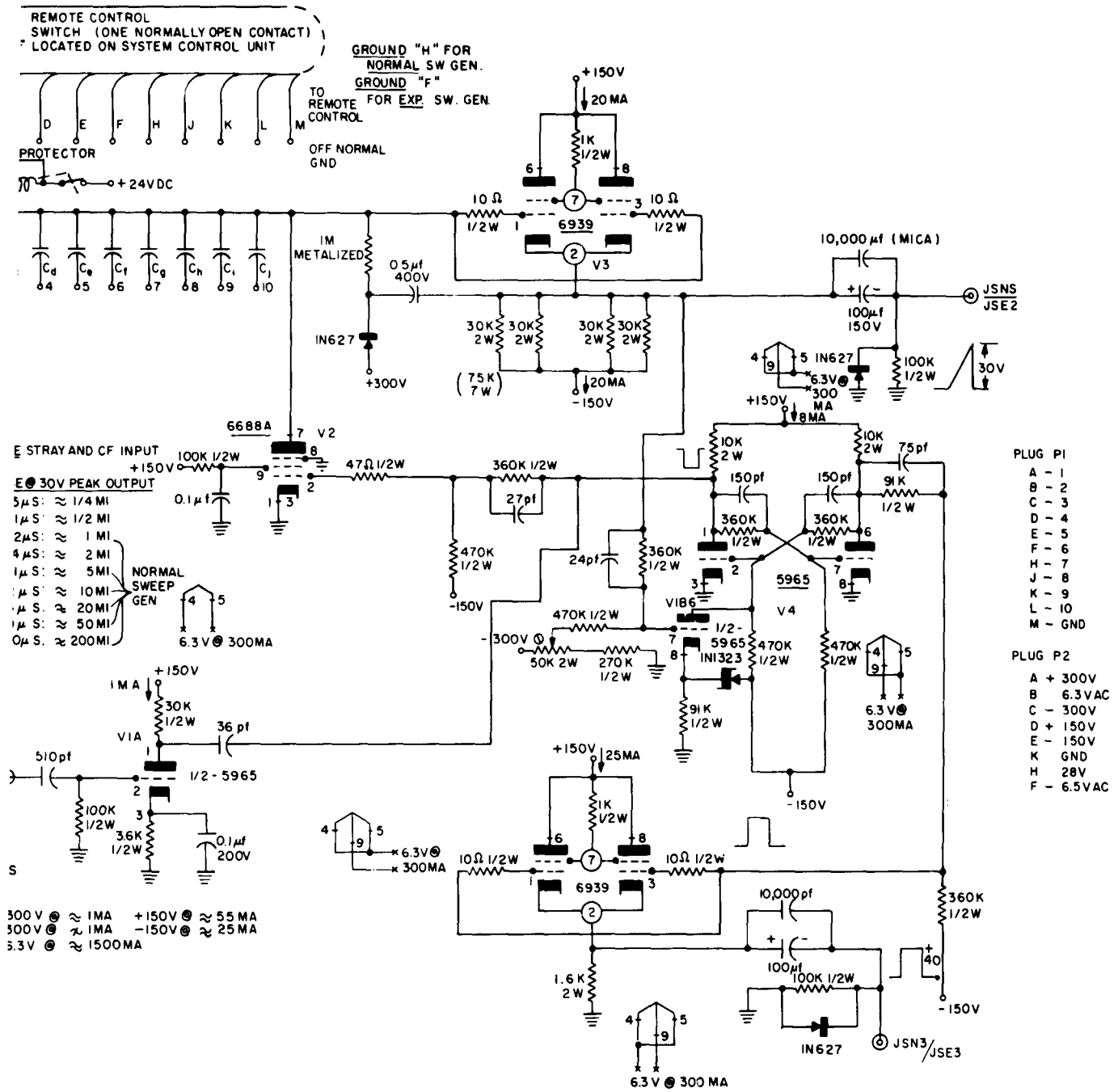

Fig. 3 - Sweep generator chassis

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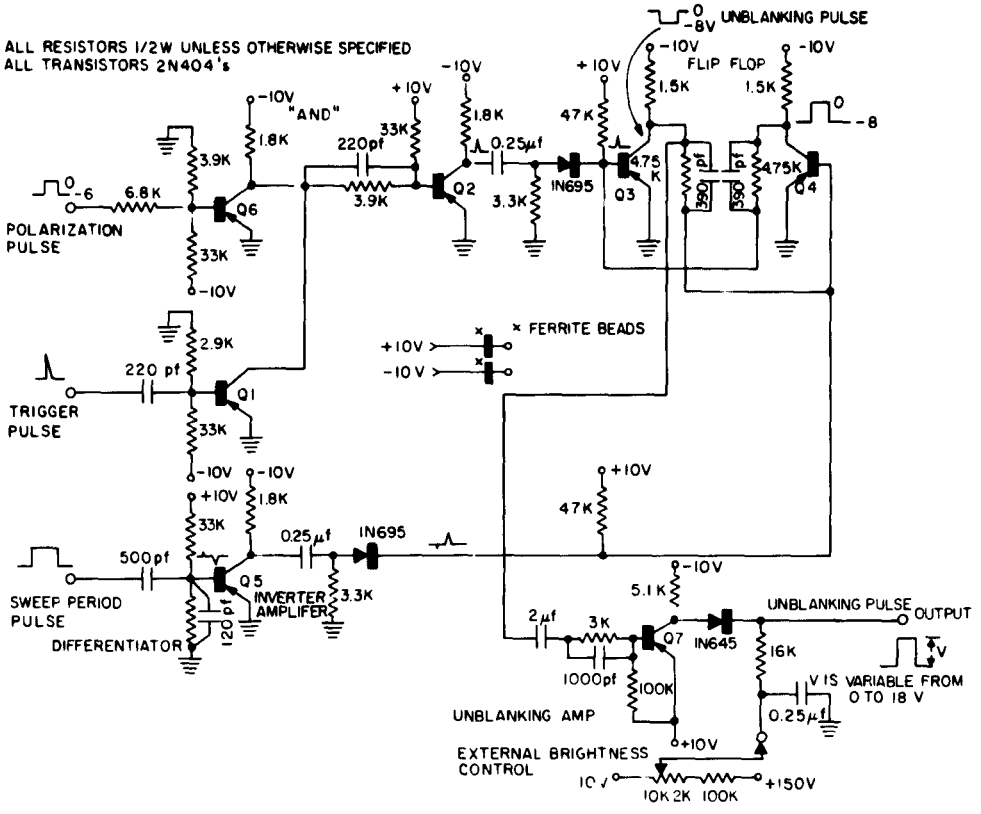


Fig. 4 - Unblanking chassis

The normal sweep is amplified and inverted by V1A. The inverted sweep is then made push-pull by the split-load phase-splitter V1B, which drives the sine-cosine potentiometer. The sine and cosine outputs are then buffered by the dual cathode follower V2. The overall gain of the resolver circuit is unity. A sine-cosine potentiometer was chosen over a standard sweep resolver because of the very large range of sweep lengths which had to be resolved for the PPI display. The sweep lengths ranged from 12.2 μs (1 mile) to 2440 μs (200 miles). No resolver system tried could satisfactorily cover this range.

PPI Deflection Amplifiers

The deflection amplifier circuit used for the PPI horizontal and vertical deflection is shown in Fig. 6. The normal sweep generator drives a Raysistor remotely controlled variable resistor which is a part of the input network. The input tube acts as a split-load phase splitter and is followed by two push-pull deflection amplifiers which are connected in an operational amplifier configuration. The final stage is capable of a ±150-volt-peak change of drive voltage at each plate and is capable of driving a 30-pf load reactance with a 12.2-μs sweep. The clamping circuits consist of dual triodes (VA and VB) which maintain the starting point of the sweeps at the center of the PPI crt. The clamping tubes are driven by amplifier VC, which receives the clamp release signal from the normal sweep period waveform. The centering controls as indicated in Fig. 1 are mounted on the front panel of the master console.

The Raysistor is a photosensitive resistor which is controlled by a built-in incandescent light. The light is controlled from the front panel by vertical gain in horizontal gain controls indicated in Fig. 1. The Raysistor photoresistor element is sensitive to large signals (within the power rating) and to ambient temperature. Also a noticeable lag occurs when the gain control is varied.

A1 and A2 Horizontal and B-Scan Vertical Deflection Amplifier

The horizontal deflection amplifiers for use with the A1 and A2 horizontal and B vertical sweeps use the circuit in Fig. 7. They are quite similar to that used for the PPI. The clamping circuits are not required, and this amplifier is offbalanced in order to take advantage of the unidirectional sweep. This amplifier can produce a 300-volt sweep of 3-μs duration at each plate of the output tube. This large voltage change is required because of the crt's low deflection sensitivity. As with the PPI sweep circuit, this deflection amplifier can drive a capacitance load of approximately 30 pf. Gain control and centering are accomplished from the front panel the same as with the PPI circuit in Fig. 6 and as shown in Fig. 1.

B Horizontal Deflection Amplifier

Because the B scope horizontal deflection is slow, the deflection amplifier is dc coupled throughout (Fig. 8). A Philbrick K2W amplifier coupled through a 1N744 avalanche diode to the phase splitting crt deflection plate driver makes up the B horizontal deflection amplifier. The gain is controlled from the front panel by a potentiometer in the feedback circuit. Front panel control of the centering is accomplished by controlling the bias of the K2W (see Fig. 1). A lower power deflection driver tube can be employed because of the low frequencies used for this deflection amplifier.

Cathode-Ray-Tube Circuit

The crt circuit is similar for all four displays as indicated in Fig. 9. The PPI and B displays use a dc restoration diode and a crt coupling capacitor is not required on the A1 and A2 displays. The only other difference is the 1090-megohm resistor used in the post accelerator of the PPI in order to reduce the geometric distortion of the display. Later measurements have shown that the 10-kilovolt postacceleration voltage on all cathode-ray tubes should be reduced to approximately 2.5 kilovolts in order to eliminate the geometric distortion caused by the crt. The unblanking signal is applied to all crt grids, while the PPI and B video drive only those respective crt cathodes.

The crt bias control is used to adjust the crt cathode-grid voltage to the proper operating region for the unblanking and video signals.

Video Amplifier PPI and B Scope

The circuit diagram in Fig. 10 is that used for both the PPI and B video displays. Provisions are made to mix the video and range marks in the dual input cathode follower VA. Range mark gain control is obtained by controlling the bias on a switching diode. The mixed video and range marks are controlled in gain by varying the dc bias on VB. The gain controls are mounted on the front panel as indicated in Fig. 1. The maximum voltage gain of the amplifier is over 30 with a rise time of approximately 30 nanoseconds while driving the crt display. The cathode follower uses shunt compensation, and the output stage uses both shunt and series compensation. By driving the crt cathode, only one stage of video amplification was required, thus avoiding the bandwidth shrinkage due to cascading amplifier stages.

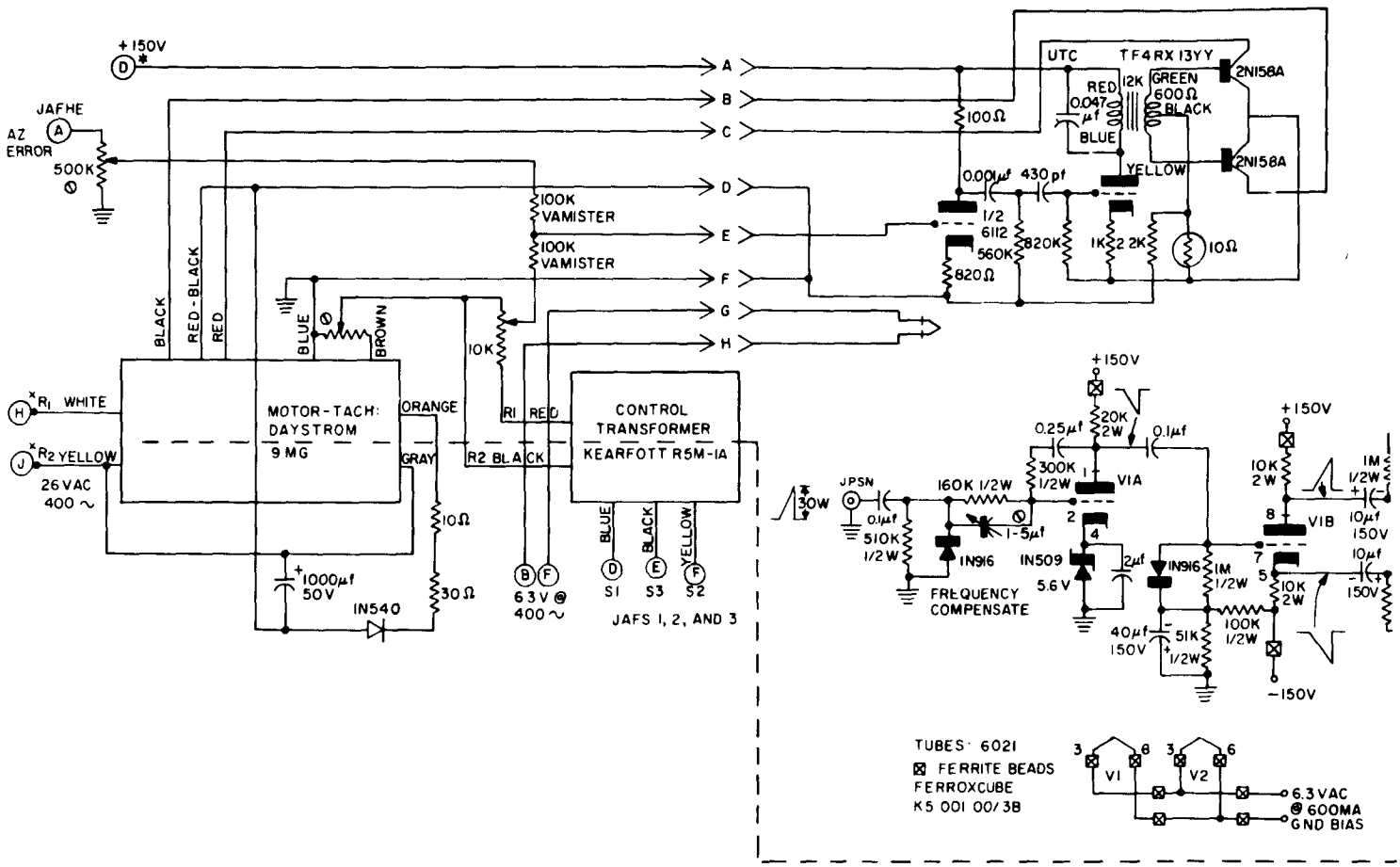


Fig. 5 - Antenna follower chassis

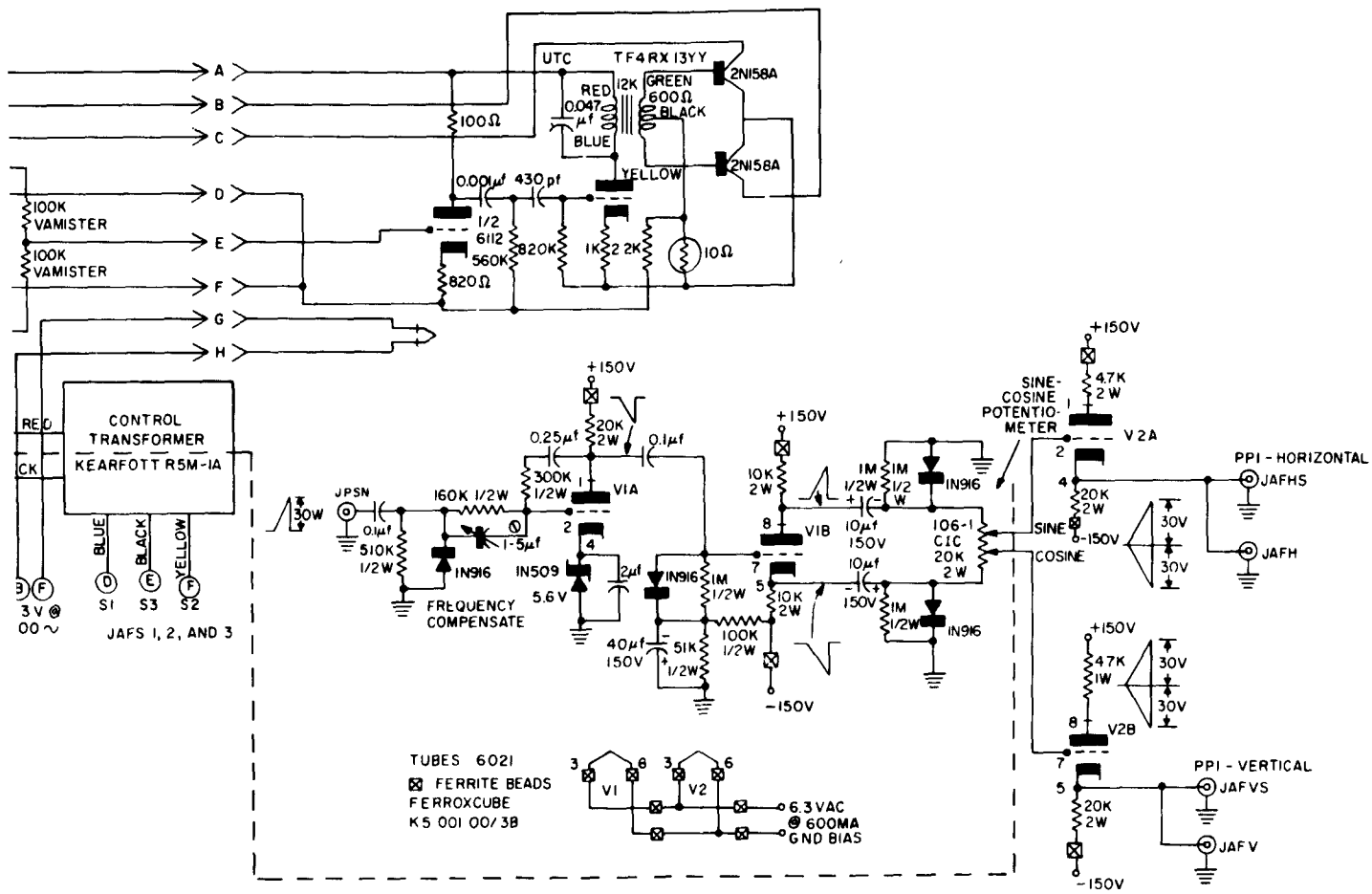


Fig. 5 - Antenna follower chassis

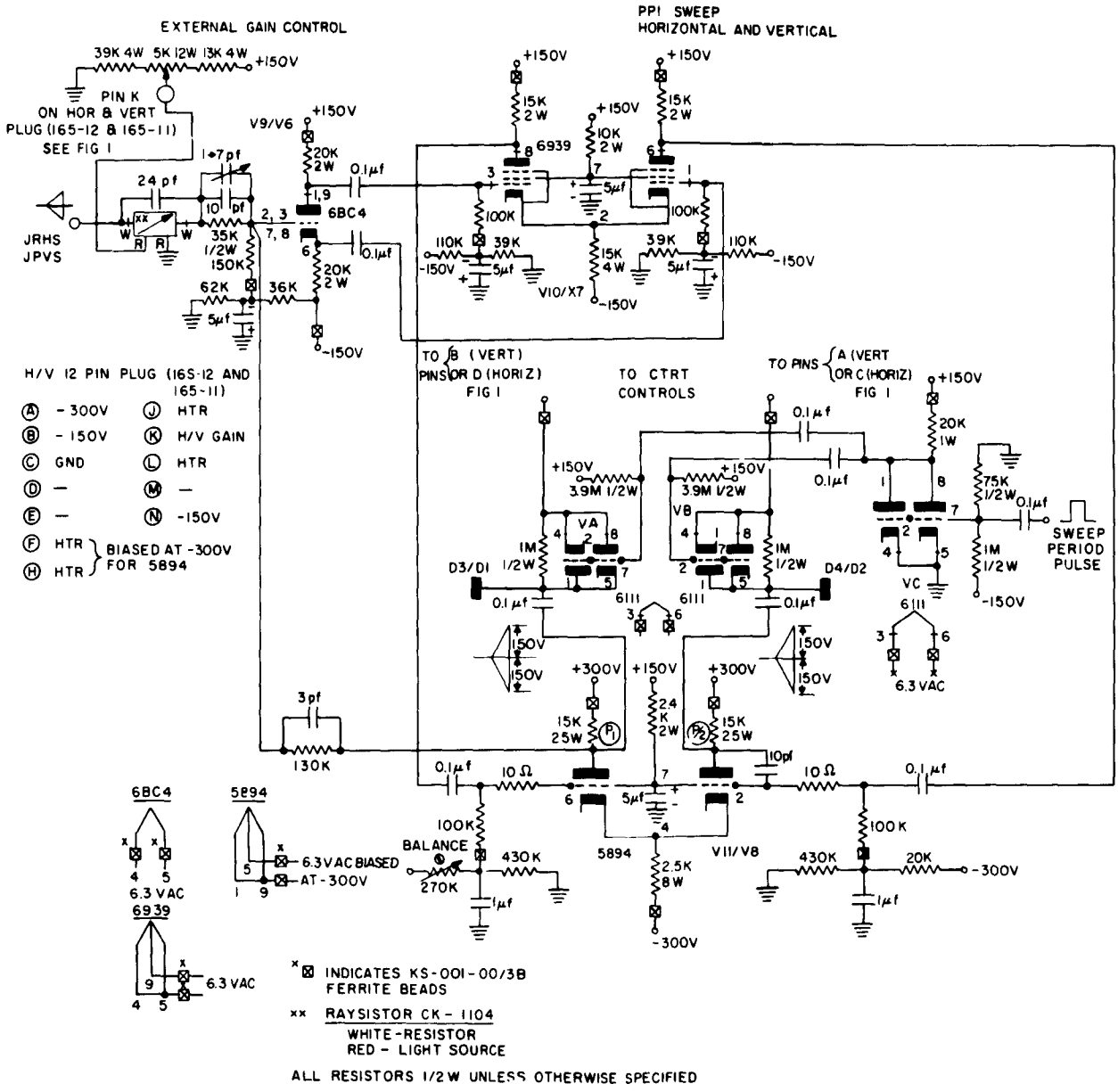


Fig. 6 - PPI deflection amplifier, horizontal and vertical

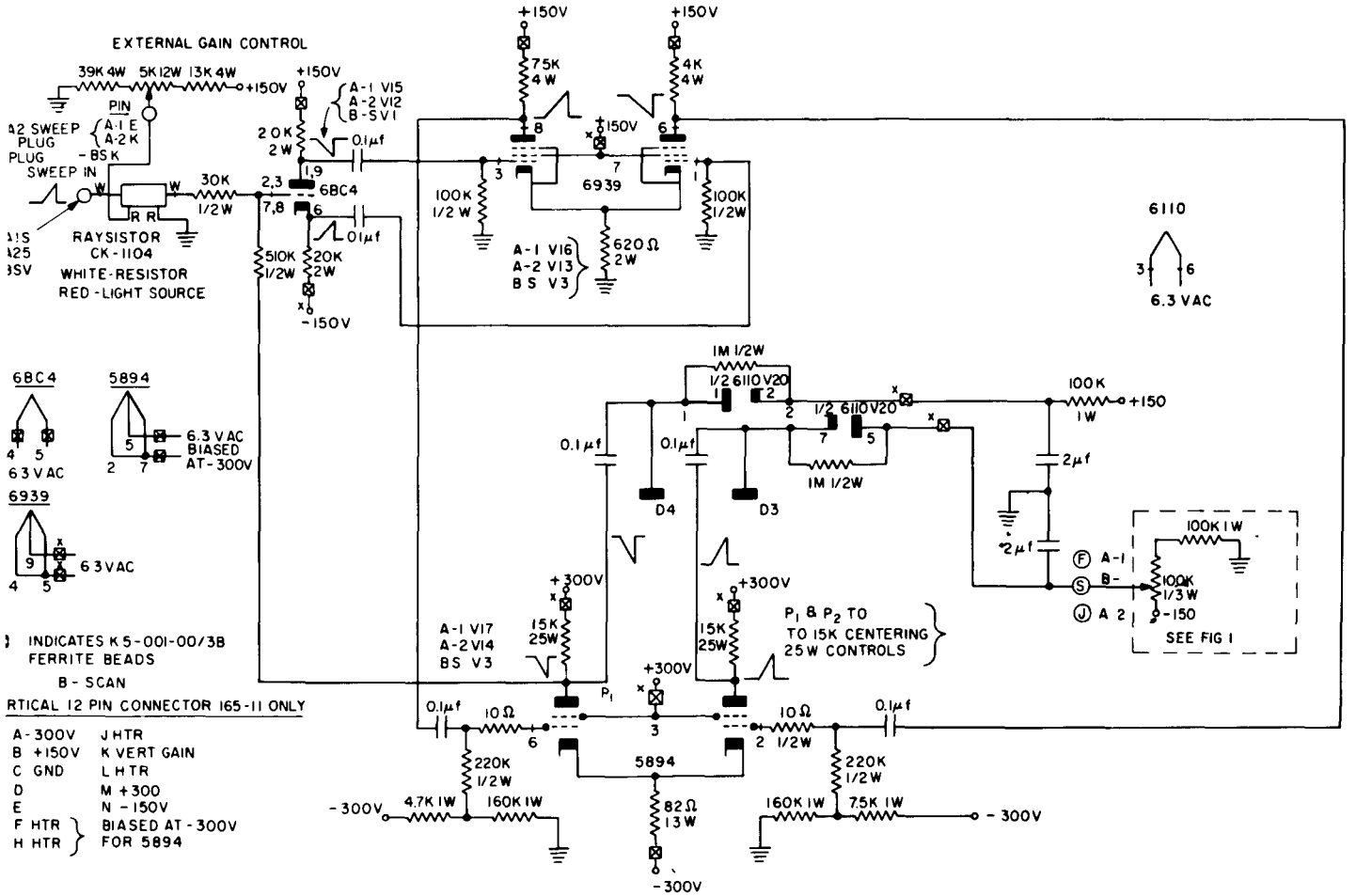


Fig. 7 - A1 and A2 horizontal and B-scan vertical deflection amplifier

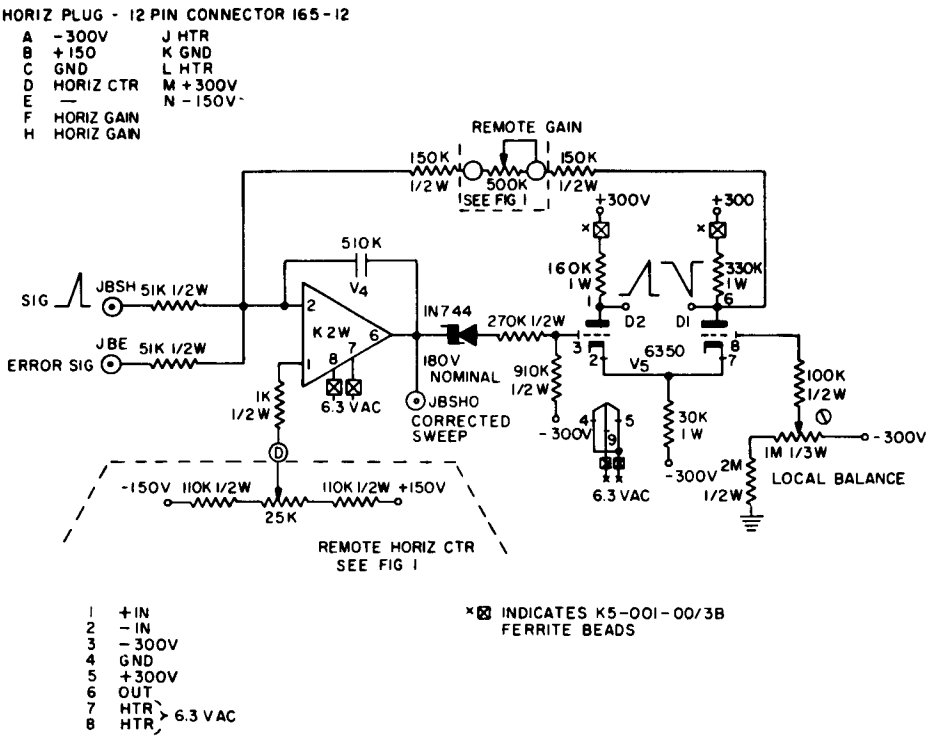
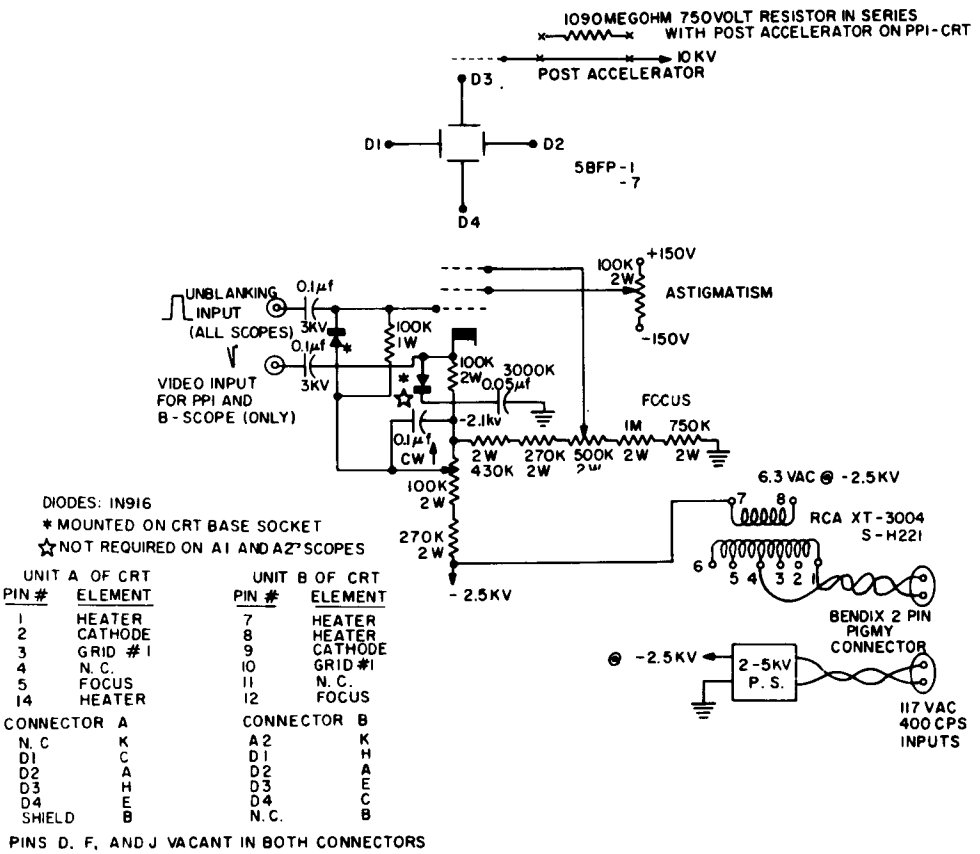


Fig. 8 - B horizontal deflection amplifier

Video Amplifier A1 and A2

The video amplifier shown in Fig. 11 for the A1 and A2 displays, in addition to displaying the video and range marks as a positive vertical deflection, must simultaneously display the gating waveforms as negative vertical deflections. The video and range mark signals are mixed and have their amplitude controlled in a similar manner as that used for the B and PPI video amplifiers. The range mark gain control is accomplished by biasing a switching diode (Fig. 11). The range mark and video signals are then mixed in the dual cathode follower V1. V1 then drives the high gain stage V2, which has a controlled bias at its grid for gain control. V2 then drives one input of the difference amplifier V3. The two gate signals are mixed at the grid of the difference amplifier V5. V5 produces a push-pull output which is used to control the final output dc restoration circuits. Also, the positive going gate signal from V5 is amplified and inverted in V6, which then drives the second input of the difference amplifier V3. Thus V3 combines the video and range marks with the gate signals in the desired manner. The dual outputs of V3 then drive the push-pull inputs of the final deflection driver stage V4. The outputs of V4 are capacitively coupled to the crt deflection plates through series compensating inductors. Centering control is accomplished from the front panel as indicated in Fig. 1. At each output, 1N916 dc restoration circuits are used. The gate amplifier inhibits these restoration circuits during the gate periods. When no gate signal is present, the diodes are biased so that they will operate as unkeyed dc restoring circuits.

Shunt compensation is used at each stage except for the dual cathode follower and gate amplifier circuits. Series compensation is used at the inputs to the final driver tube.



UNIT A OF CRT		UNIT B OF CRT	
PIN #	ELEMENT	PIN #	ELEMENT
1	HEATER	7	HEATER
2	CATHODE	8	HEATER
3	GRID #1	9	CATHODE
4	N. C.	10	GRID #1
5	FOCUS	11	N. C.
14	HEATER	12	FOCUS

CONNECTOR A		CONNECTOR B	
N. C	K	A2	K
D1	C	D1	H
D2	A	D2	A
D3	H	D3	E
D4	E	D4	C
SHIELD	B	N.C.	B

PINS D, F, AND J VACANT IN BOTH CONNECTORS

Fig. 9 - Cathode-ray-tube circuit

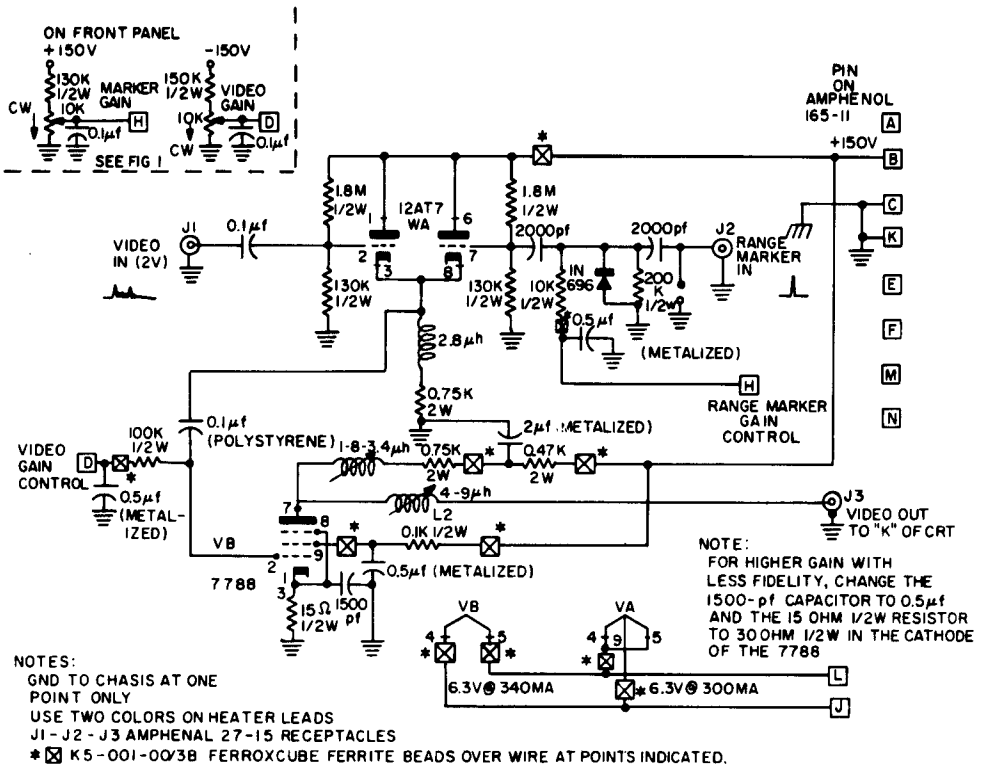


Fig. 10 - PPI and B-scope video amplifier

The video amplifier has a voltage gain from the input to one of the outputs of approximately 30. The output rise time is approximately 30 nanoseconds while driving the crt vertical deflection plate network. With the 5BFP cathode-ray tubes, this circuit has a capacitance loading of approximately 25 to 30 pf and a sensitivity of approximately 45v/cm. The output circuits driving the deflection plates are similar to those described by Thirup.*

Master Console Control Circuits

The various control circuits used in the four-frequency radar are located in the master console. These circuits are shown in brief form in Fig. 12 indicating their terminations either in the master console main junction box or at the contractor's terminal board indicated. Explanation of these circuits will be detailed by the contractor. Sufficient information is presented here to indicate the circuits which allow the radar displays to be turned off independently of the rest of the system. When the receiver filament ON switch is operated, the relay controlling the 400-cps ac to the console displays is energized. This in turn activates the heater supply transformer chassis shown in Fig. 13. Power is also made available to the master console plate supply switch. When this switch is operated, all of the dc power is made available to the master console through the dc power relay. When the dc power relay operates, the HV relay on Fig. 12 operates and supplies ac voltage to the high voltage crt power supplies. A manually operated toggle switch at the rear of the crt frame is placed in series with the HV relay contacts so that the crt high voltages may be turned off independently of the dc power relay.

*G. Thirup, "Design of Low-Pass Amplifiers for Fast Transients," Philips Research Reports 10:216 (1955).

Master Console Configuration

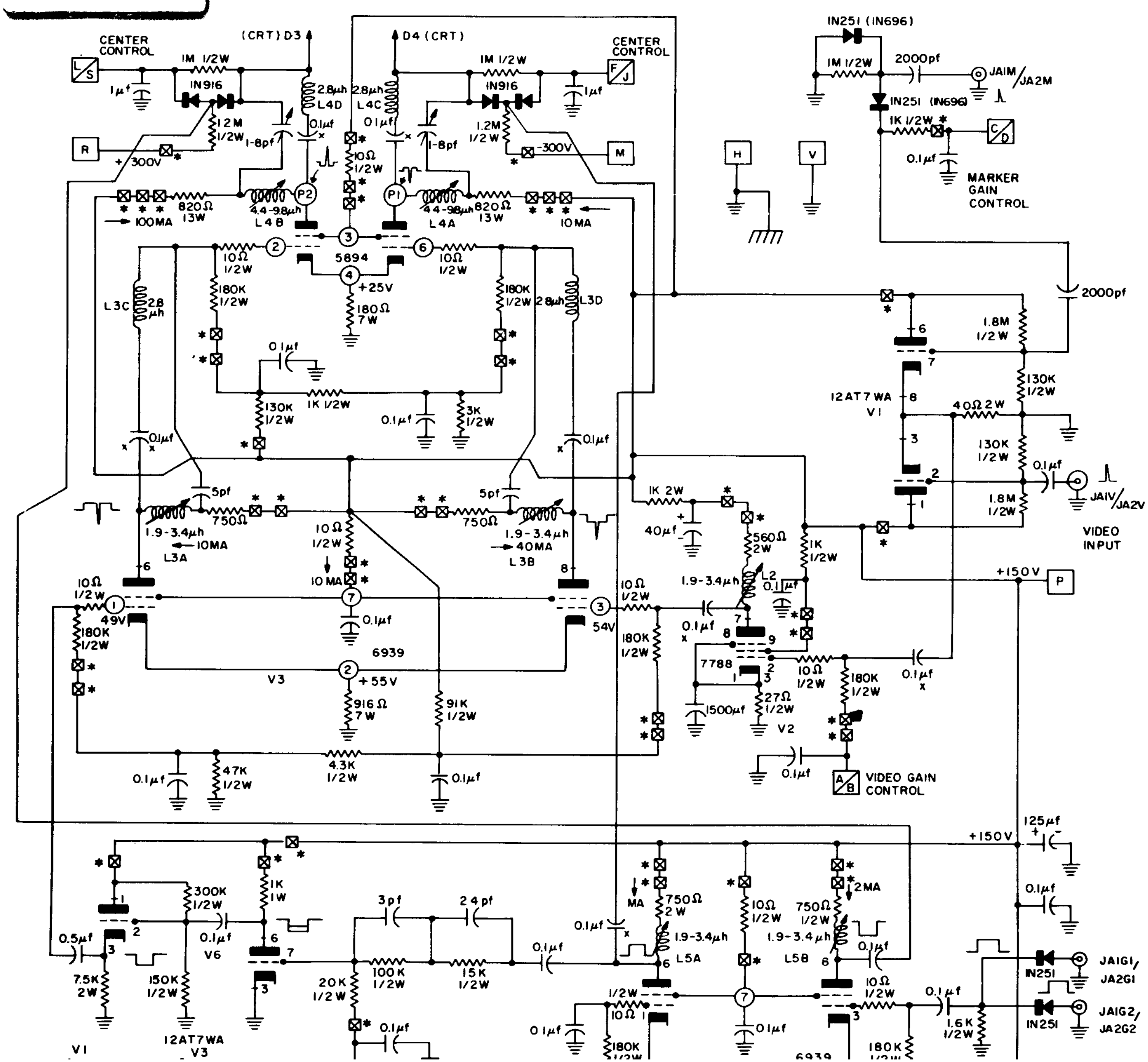
Figures 14 through 20 are pictures of the master console immediately before painting and shipping to the four-frequency radar contractor. These pictures were made after the console had been cleaned up and rechecked after the fire mentioned in the Introduction. Figure 14 shows a front view of the crt display. The upper right side of the console is shown in Fig. 15, while the upper rear view is pictured in Fig. 16. The large chassis in the center contains the A1 and A2 sweep and video amplifiers. The small projecting side chassis on each side and supporting the main chassis, contain the B (on the left) and the PPI (on the right) sweep amplifier circuits. The B and PPI video amplifiers are mounted on the small chassis above their respective cathode-ray tubes. The two sweep generator chassis are shown at the bottom of Fig. 16. The sweep control relays are mounted behind and to the left of the sweep generators. The high voltage control relay is mounted on the shelf at the front and to the left of the sweep generators. Figure 17 shows the lower rear of the master console. The delayed trigger separator chassis has been eliminated and is not used. Figure 18 is a front view of the bottom of the master console without the contractor's chassis. Figure 19 pictures the top of the master console before the system control unit is mounted on the console. The main junction box is shown in Fig. 20. The dc power relays are mounted on the left side and the ac power relay is mounted near the bottom left corner.

PERFORMANCE

The completion of the design and construction of the four-frequency radar master console was undertaken at NRL. The delivery of the master console by NRL to the contractor on schedule was delayed by damage incurred by a fire in the truck carrying the console to the contractor's plant. The damaged console was restored to operating condition and delivered to the contractor after six working days.

When the master console was delivered to NRL, it had been partially laid out and wired. The portion of the work done at the contractor's plant was continued where practical. The video amplifiers were redesigned and relocated in the console in order to meet the bandwidth and operational requirements. The sweep generators and sweep amplifiers were redesigned in order to provide 1/4- to 200-mile sweeps. Figure 21 shows the PPI display with a 1-mile sweep range and a 0.1-μs pulse. Figure 22 shows two views of the A1 and A2 displays, with time advancing from the right. The top A1 display shows a 0.1-μs half-sine pulse on a 1/4-mile sweep and the top A2 display shows a 0.1-μs half-sine pulse on a 1-mile sweep. The bottom view shows the reverse of the top. Geometric distortion can be seen in this picture. Figure 23 shows two views of the B display, with time advancing from the bottom. The figure shows the 0.1-μs half-sine pulse on the 1-mile sweep at the top and on the expanded 1/4-mile sweep at the bottom.

The video and trigger coaxial leads were wired to wafer switches by the contractor as indicated in Fig. 1. This caused improper termination of these lines when the coaxial leads from the switch to the various chassis were installed. In the case of the trigger line, additional loading at the final termination beyond the diode adding network was added until proper operation was obtained. In the case of the video lines, amplitude and some phase distortion is encountered as the various amplifiers are switched through the various positions. Later determination showed that the 10 kv chosen by the contractor for the post-accelerator was too high and caused geometric distortion of the displays (see Fig. 22). The cathode-ray tubes chosen by the contractor were found to have a combination of low deflection sensitivity and high input capacitance (between 20 and 30 pf) thus increasing the difficulty in obtaining the desired sweep and video bandwidths. The bandwidths were obtained only at great expenditure of power in these circuits. These cathode-ray tubes defocused severely a short distance (approximately 3 cm) from the center. The Raysistor units used to control the sweep gain remotely were found to be excessively temperature sensitive and to have too long an operation lag for this purpose. The units were also found to be sensitive to larger signal voltages even though being operated within their rated limits.



(CRT) D3
D4 (CRT)
CENTER CONTROL
L/S
F/J
R
M
H
V
C/D
A/B
P
1M 1/2W
IN916
12M 1/2W
1.2M 1/2W
+300V
-300V
1μf
1-8pf
2.8μh L4D
2.8μh L4C
0.1μf
10Ω 1/2W
4.4-98μh L4B
4.4-98μh L4A
820Ω 13W
100MA
10MA
5894
+25V
180Ω 7W
180K 1/2W
130K 1/2W
1K 1/2W
3K 1/2W
L3C 2.8 μh
2.8μh L3D
5pf
750Ω
1.9-3.4μh
L3A
L3B
40MA
49V
54V
6939
V3
+55V
916Ω 7W
91K 1/2W
4.3K 1/2W
47K 1/2W
IN251 (IN696)
2000pf
JAIM/JA2M
IK 1/2W
MARKER GAIN CONTROL
1.8M 1/2W
12AT7WA
V1
40Ω 2W
JAIV/JA2V
VIDEO INPUT
+150V
1K 2W
40μf
560Ω 2W
L2
7788
1500μf
27Ω 1/2W
V2
VIDEO GAIN CONTROL
125μf
300K 1/2W
1K 1W
0.5μf
7.5K 2W
150K 1/2W
V6
3pf
24pf
100K 1/2W
15K 1/2W
20K 1/2W
750Ω 2W
L5A
L5B
MA
2MA
JAIG1/JA2G1
JAIG2/JA2G2
IN251
1.6K 1/2W

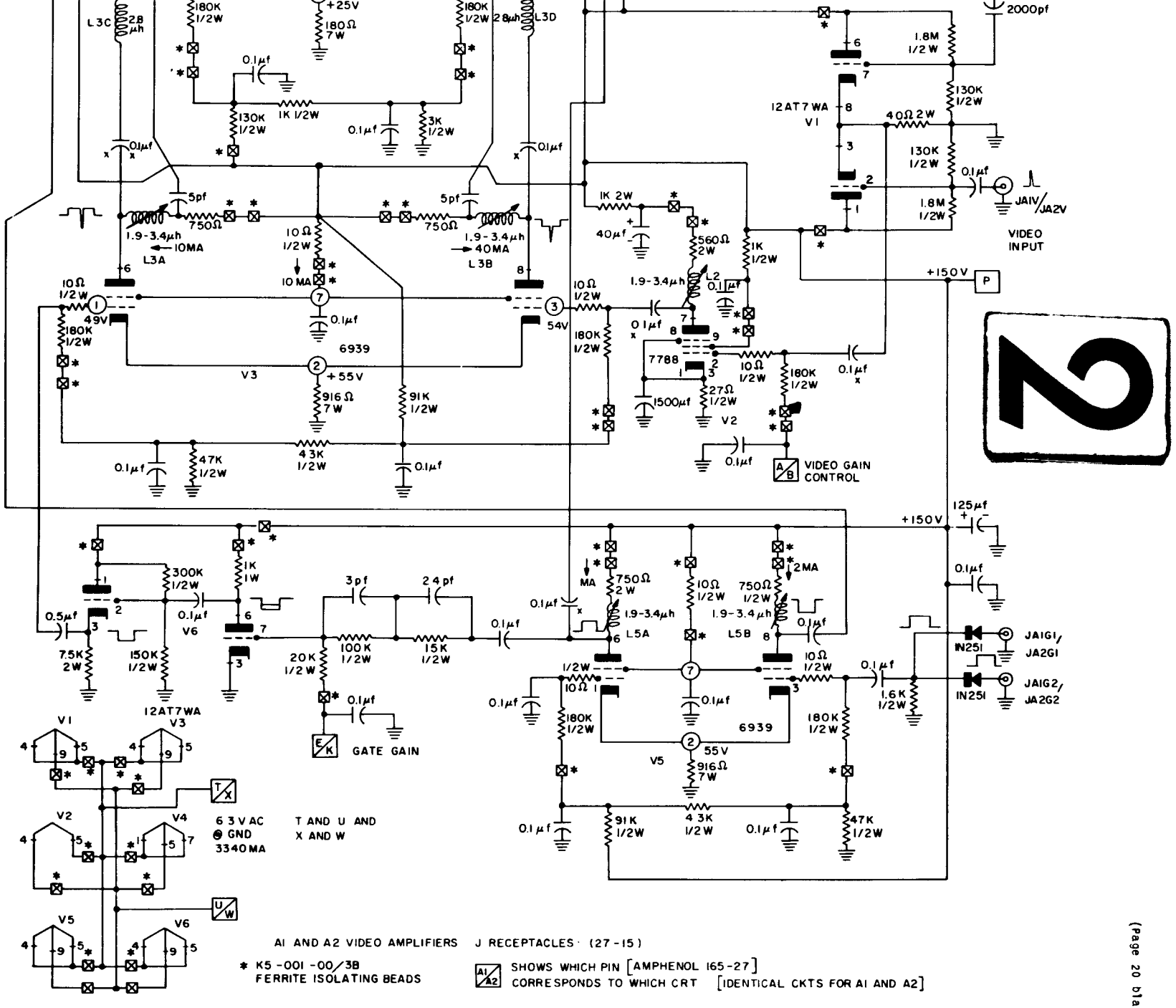


Fig. 11 - A1 and A2 video amplifier

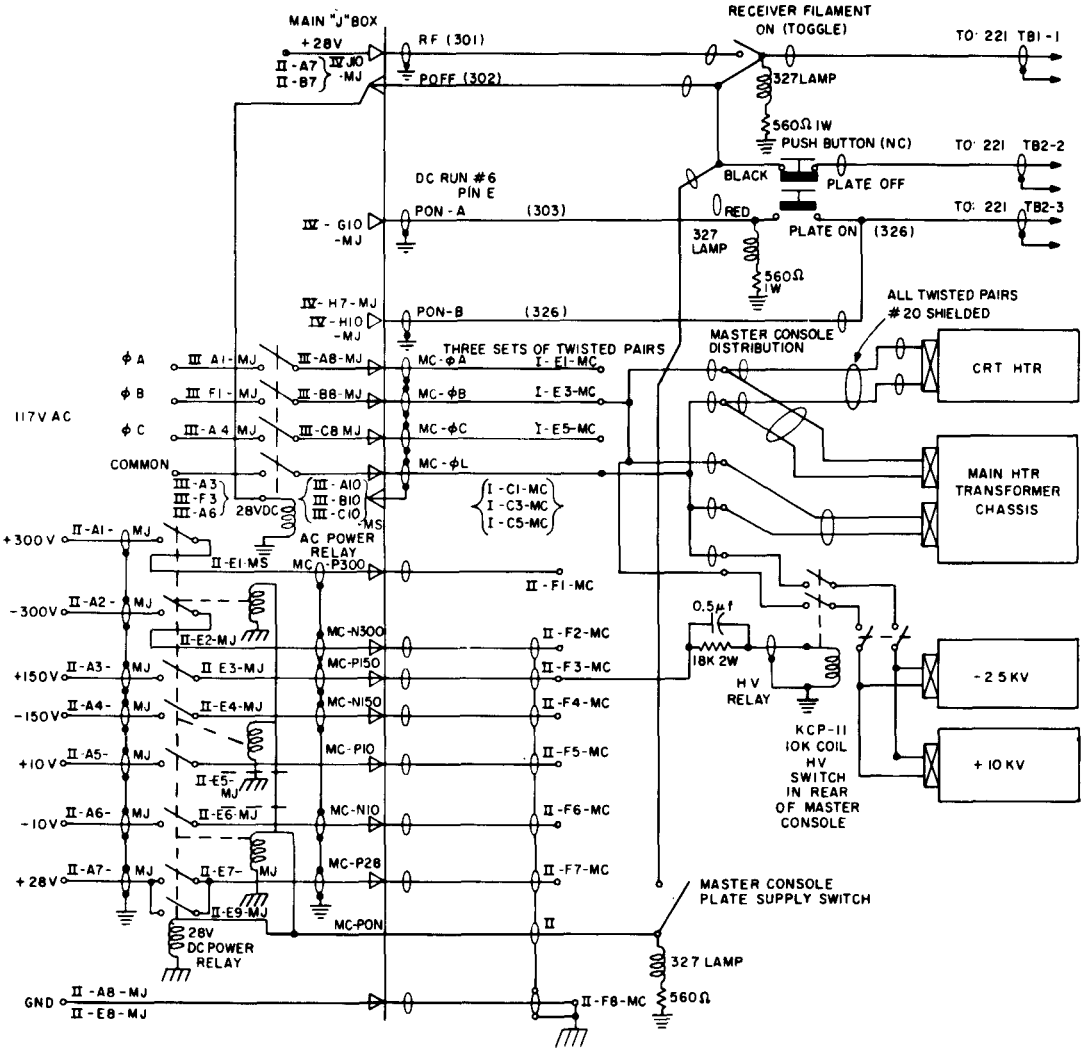


Fig. 12 - Master console control

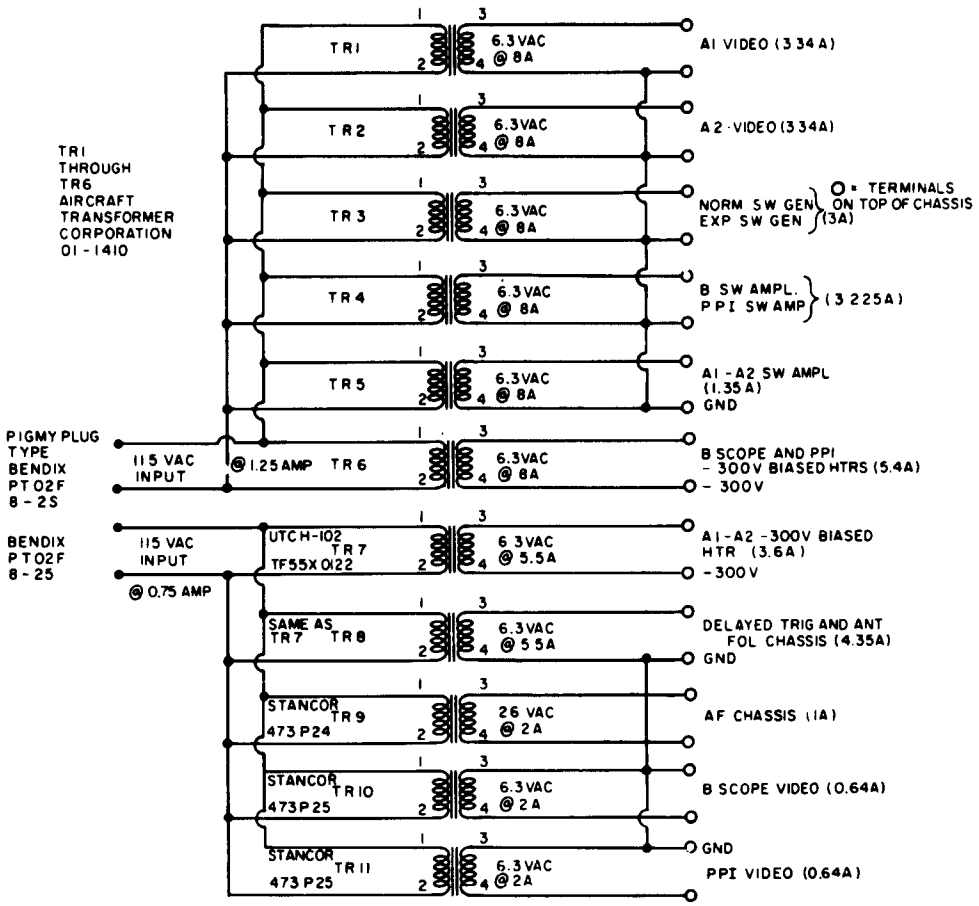


Fig. 13 - Heater supply chassis

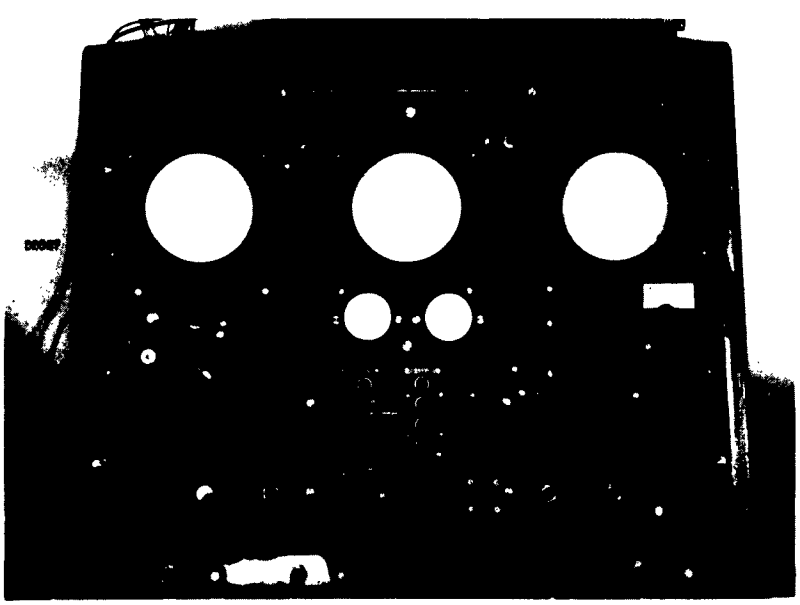


Fig. 14 - Front panel of the master console

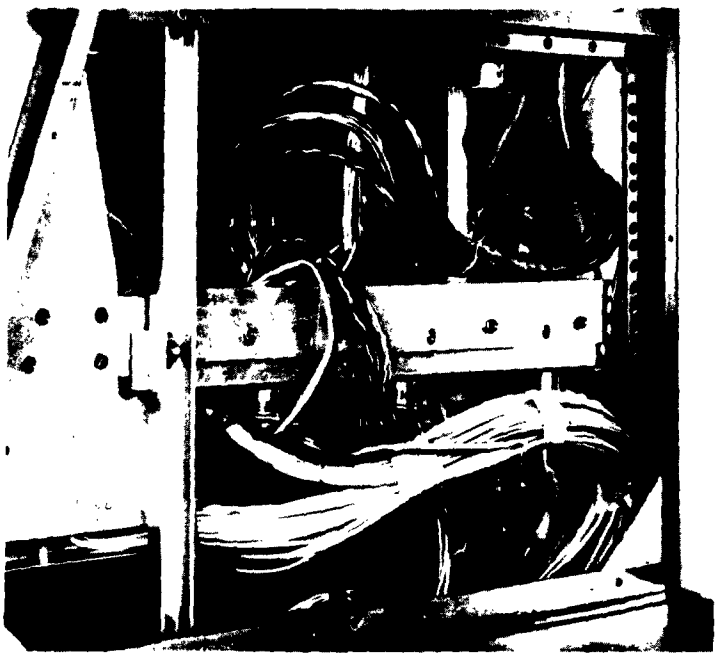


Fig. 15 - Upper right side of the master console

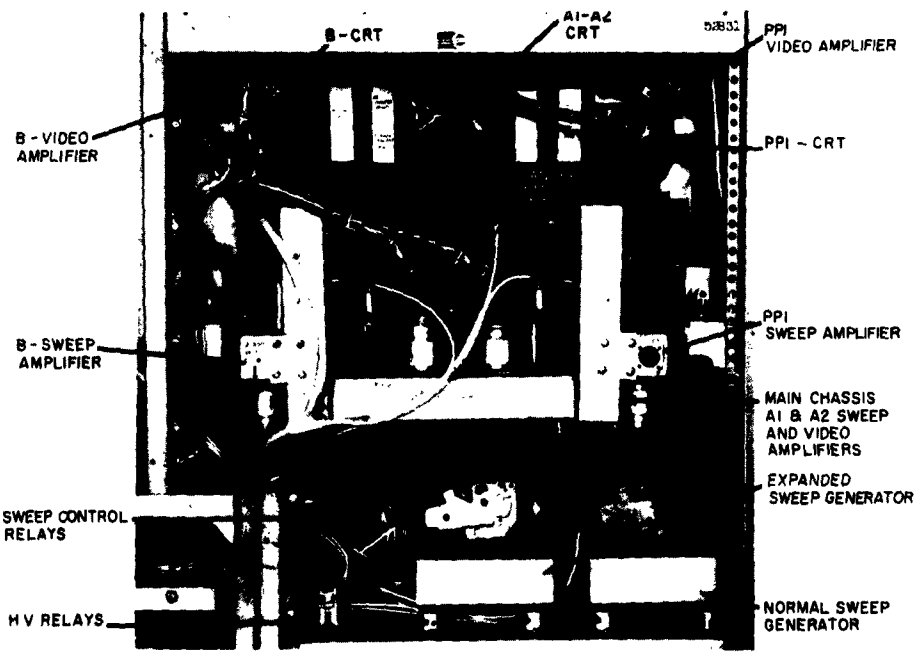


Fig. 16 - Upper rear of the master console

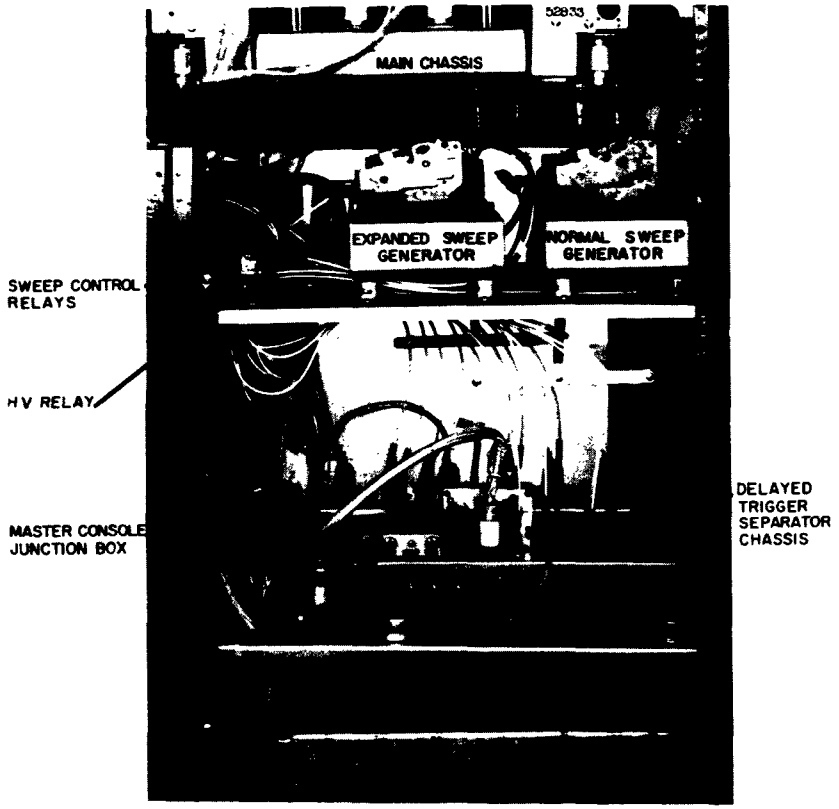


Fig. 17 - Lower rear of the master console

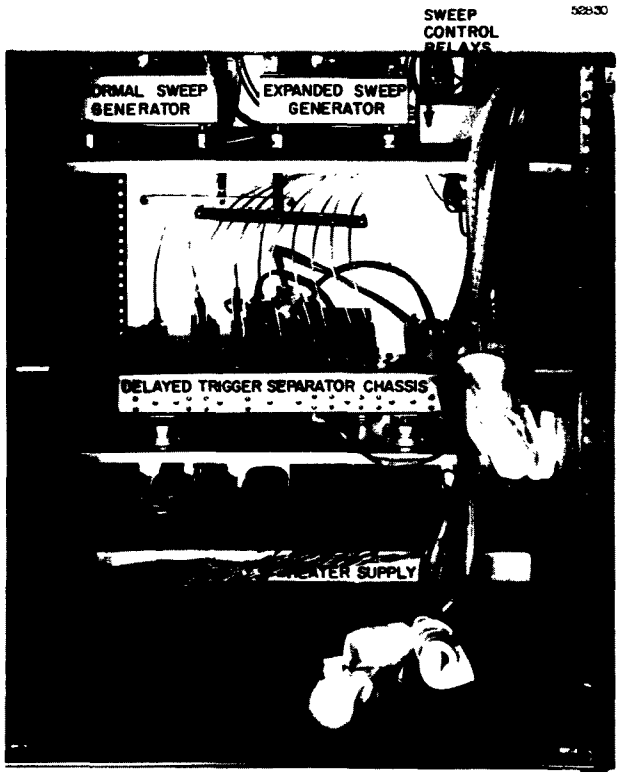


Fig. 18 - Lower front of the master console

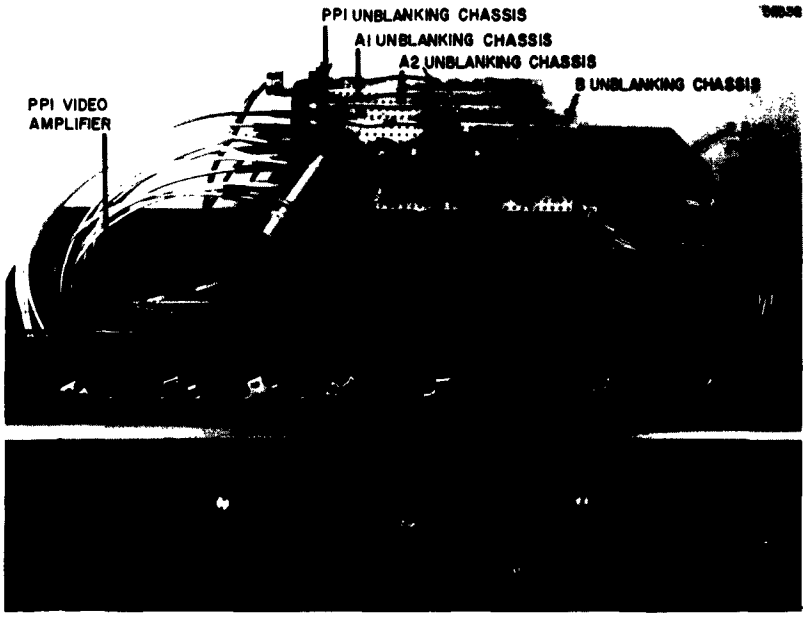


Fig. 19 - Upper front of the master console

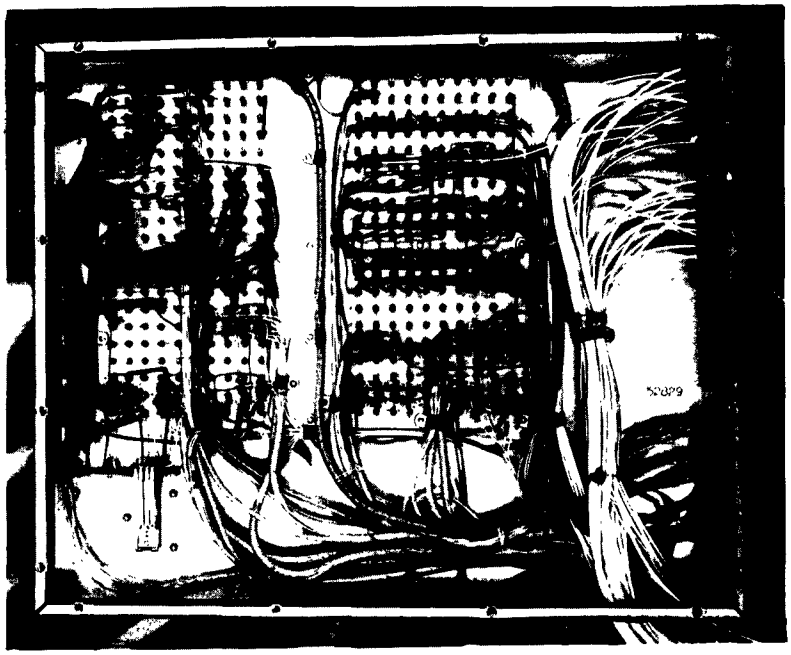


Fig. 20 - Main junction box

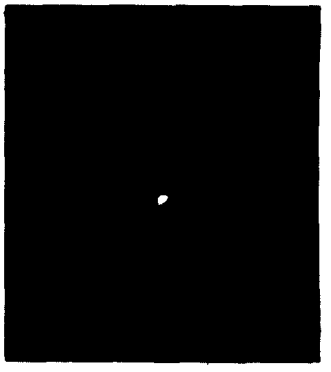


Fig. 21 - Master console PPI display with a 1-mile sweep and a 1-μs pulse

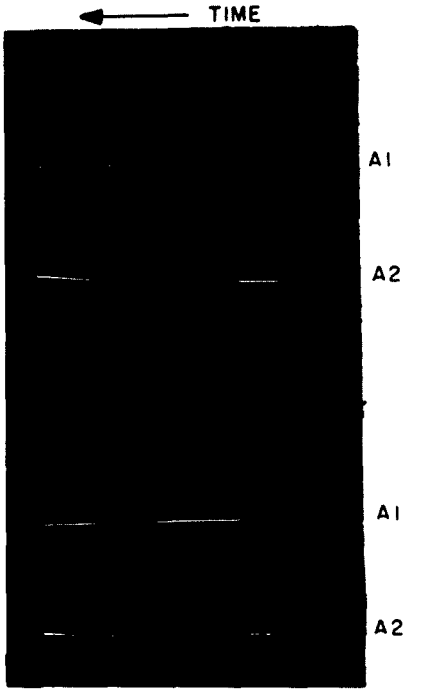


Fig. 22 - Master console A1 and A2 display with a 0.1-μs pulse on a normal 1-mile sweep (A2 top and A1 bottom) and on an expanded 1/4-mile sweep (A1 top and A2 bottom)

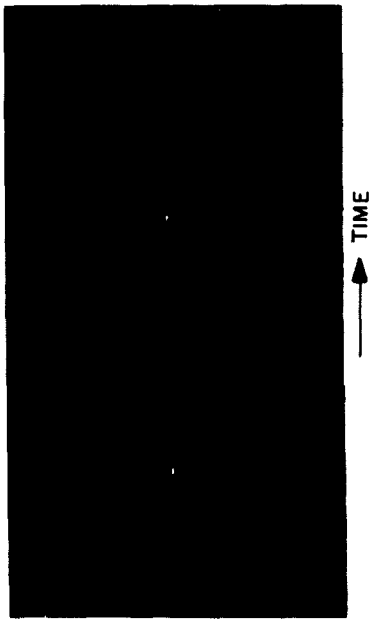


Fig. 23 - Master console B display

RECOMMENDATIONS

The present cathode-ray tubes should be used for the PPI and B displays only. The postaccelerator voltage should be reduced in order to eliminate the crt geometric distortion. Dynamic focusing techniques should be incorporated so that a larger portion of the crt display can be used. The A1 and A2 cathode-ray tube should be replaced by one having a greater deflection sensitivity and a lower deflection capacitance.

The major recommended change is to replace the coaxial wiring for the video and trigger lines with selection relays and buffer amplifiers in the main junction box. This would eliminate all interaction due to mismatch and loading. This would require a total of eleven coaxial lines interconnecting the junction box and the main console. All of the fragile wiring of the RG-195/U coaxial cable to the wafer switches would be eliminated.

Modular construction should be used throughout the console where practical. The gain controls should not use temperature sensitive elements or, in the case of the video amplifier, vary the transconductance of a tube.

FUTURE WORK

For consoles 2 and 3, the method of using dynamic focusing of the cathode-ray tubes will be determined and the crt for the A1 and A2 display will be selected. Modular slide-in units will be designed for the various functions and the overall console layout modified for easier maintenance. Video-type relays will be selected for the trigger and video switching functions. Transistorized circuits will be used except where vacuum tubes provide superior performance. All vacuum tubes used except for the final deflection drivers will be premium ruggedized subminiature tubes. The transistors used will be silicon, so that effects of environmental temperature extremes may be avoided. The video gain control will be through 100-ohm poteniometers which will terminate the coaxial line. This will avoid a variation of bandwidth with gain as happens when a tube transconductance is varied for gain control. Gain control in the deflection amplifiers will be done by varying the feedback resistance in these amplifiers.

The dc restoration used in the A1 and A2 video amplifiers will be changed so that the unblanking waveform inhibits the restoration circuit instead of the gating pulse. The clamping circuit on the PPI will be released by the pretrigger so that switching transients at the center of the PPI display can be avoided.

ACKNOWLEDGMENTS

The author wishes to express appreciation for the contributions, efforts, and assistance given by the members of the Combined Systems Section: to Mr. D. J. McLaughlin, who is head of the section, to Mr. S. C. Wardrip for his work on the deflection circuits and all the other assistance he provided, and to Mr. L. Werling for his efforts in getting the master console constructed.

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Naval Research Laboratory. Report 5922. FOUR-FREQUENCY RADAR MASTER CONSOLE, by F.R. Fluhr, 28 pp. and figs., June 7, 1963.

In conjunction with the commerically contracted development of the airborne four-frequency radar system to be used in the Laboratory's wave propagation studies, the master console design was assumed by NRL. Four displays were incorporated into a single console, along with transmitter, receiver, and antenna drive control functions. Two cathode-ray tubes present the PPI and B scans, while a third presents dual traces representing linear A sweeps. The system-control-panel-assembly portion of the master console was completed on schedule to assist the contractor in the radar development. The rest of the console was designed and

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